What is claimed is:

1. An apparatus for controlling a bank refresh including a plurality of banks, comprising:

5   a plurality of input buffer means for buffering bank address signals inputted from an external circuit with the command signal;

a counter for producing count signals, being reset by an output signals from the N input buffer means;

a switch means for combining the count signals from the counter in order to

10   produce internal bank refresh signals in response to bank address signals from the N buffer means; and

a chipset control means for generating a plurality of internal bank addresses for the refresh using the internal bank refresh signals.

15   2. The apparatus as recited in claim 1, wherein the number of the plurality of banks is 2^N, the number of the plurality of input buffer means is N and the counter is (N-1)-nary.

3. The apparatus as recited in claim 2, wherein the N input buffer means

20   includes a latch means for sustaining the output signals of the N input buffer means within a certain period of time only when the refresh command signals are applied.

4. The apparatus as recited in claim 2, wherein the (N-1)-nary counter is reset by a logic combination of the bank address signals.

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5. A method for controlling a bank refresh including 2^N of banks, comprising the steps of:

    a) buffering N bank address signals inputted from the external circuit with the refresh command signals;

5   b) outputting the (N-1)-nary count signal in sequence by resetting at least one of N buffered signals;

    c) switching and outputting unit of N-1 count signals to the bank refresh combination signals in response to the N buffered signals; and

    d) generating an internal bank address for the refresh using the bank refresh

10 combination signals.